Abstract of the Disclosure

A non-volatile memory device includes an array of non-volatile memory cells. The memory has control circuitry to erase the non-volatile memory cells and perform erase verification operations. The memory can be arranged in numerous erasable blocks and/or sub-blocks. An erase register stores data indicating an erase state of corresponding memory sub-blocks. During erase verification, the memory programs the erase register when a non-erased memory cell is located in a corresponding sub-block. Additional erase pulses can be selectively applied to sub-blocks based upon the erase register data. Likewise, erase verification operations can be selectively performed on sub-blocks based upon the erase register data. An address register is provided to store an address of a non-erased memory cell identified during verification. The address from the register is used as a start address for subsequent verification operations on the same array location.